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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/122,349	07/24/1998	LANCE HACKING	042390.P5965	4301

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EXAMINER	
TRAN, DENISE	

ART UNIT	PAPER NUMBER
2186	15

DATE MAILED: 12/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/122,349	Applicant(s) HACKING ET AL.	
	Examiner Denise Tran	Art Unit 2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-12 and 38-64* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-12 and 38-64* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 July 1998* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. In response to the applicant's requests during the telecommunication on 03/08/01, claims 13-37 have been rejoined as new claims 42-64, the restriction requirement made in Paper No. 3 is hereby withdrawn.

2. Claims 1-12 and 38-64 are presented for examination. Claims 3 and 13-37 have been canceled.

3. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: "execution unit shifts the data elements by a predetermined . . . invalidated" claim 5, lines 1-3; "execution unit further invalidates data . . . " claim 12, lines 1-3; Claims 11 and 40 have the similar problems as discussed in claims 5 and 12.

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "execution unit shifts the data elements by a predetermined . . . invalidated" claim 5, lines 1-3; "execution unit further invalidates data . . . " claim 12, lines 1-3; Claims 11 and 40 have the similar problems as discussed in claims 5 and 12, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-2, 4-12, and 38-64 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rahman et al., U.S. patent No. 5,778,431, (hereinafter Rahman) in view of Milburn et al. U.S. Patent No. 5,524,233 (hereinafter Milburn).

As per claims 1, 7, 38, 42, 46, 51, 56 and 62-63, Rahman teaches the invention substantially as claimed, comprising: a first storage area to store data (e.g., fig. 1, el. 114); a cache memory having a plurality of cache lines, each of which stores data (e.g., fig.1, el. 106 and col. 5, line 27 and et seq.); a second storage area to store instructions (e.g., col. 7, line 22 and et seq.); and an execution unit coupled to the first storage area, the second storage area, and the cache memory to operate on data elements identifying a user-definable or physical address (e.g. col. 3, lines 25-30, col. 5, lines 30-35 and col. 7, lines 25-28) to invalidate data in a predetermined portion of the plurality of

cache lines in response to receiving an instruction (e.g., col. 7, line 22 and et seq.) or copy data in a predetermined portion of the plurality of cache lines to the first storage area in response to receiving an instruction (e.g., col. 7, line 22 and et seq.); or a processor comprising a circuit to obtain a user specified starting address (e.g., col. 3, lines 25-35 or abstract) of a predetermined area of the cache memory (e.g., fig.1, els. 101 or 102) by reading a portion of an address in a register specified in the code (e.g. col. 7, lines 24-28) and invalidate data in the predetermined area of cache memory (e.g., col. 7, line 22 and et seq.) or copy data from the predetermined are of cache memory and store the copy data in the storage area separate from the cache memory (e.g., col. 7, line 22 and et seq.) and a portion of a starting address of the cache line in which data to be invalidated or copied (i.e., tag address; e.g., col. 7, line 22 and et seq.). Even though Rahman teaches the use of validation being implemented through instruction in the CPU micro code stored in ROM and operating address values to invalidate or copy data (e.g., col. 7, line 22 and et seq.) but does not specifically show the use of providing a single instruction with an operand and decoder to decode an instruction. Milburn shows providing a single instruction with an operation code and address values in its operand (e.g., col. 9, lines 1-10; col. 10, lines 10-15; and col. 11, lines 1-20) are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a single instruction with an operation code and address values in its operand to Rahman's system because it would allow an instruction to influence multiple lines in a cache, invalidating an entire cache range, thereby reducing overall operation times. Milburn

shows a decoder to decode an instruction (e.g., fig. 2, line 203) are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a decoder to Rahman's system because it would produce an operation and a address values of an instruction and it would allow an instruction to influence multiple lines in a cache, invalidating an entire cache range, thereby reducing overall operation times.

As per claims 2, 4, 6, 8-9, 11-12, 39, 41, 43, 45, 47, 49-50, 52, 55, 57, 60-61, and 64, Rahman shows a register address values (i.e., a memory register address; e.g., col.7); a portion of a starting address of the cache line in which data to be invalidated or copied (i.e., tag address; e.g., col. 7, line 22 and et seq.); the portion of a starting address including a plurality of most significant bits of the starting address (i.e., tag address; e.g., col. 7, line 22 and et seq.); the predetermined portion of the plurality of cache lines is a page in the cache memory (i.e., a page can be a cache line; e.g., col.7); an execution unit coupled to the first storage area, the second storage area, and the cache memory to operate on data elements to invalidate data in a predetermined portion of the plurality of cache lines in response to receiving an instruction (e.g., col. 7, line 22 and et seq.) or copy data in a predetermined portion of the plurality of cache lines to the first storage area in response to receiving an instruction (e.g., col. 7, line 22 and et seq.); and setting an invalid bit corresponding to the predetermined area of cache memory (e.g., col. 5, line 40 and et seq.) . Even though Rahman teaches the use of validation being implemented through instruction in the CPU micro code stored in ROM and operating address values to invalidate or copy data (e.g., col. 7, line 22 and

et seq.) but does not specifically show the use of providing a single instruction with an operand and decoder to decode an instruction. Milburn shows providing a single instruction with an operation code and address values in its operand (e.g., col. 9, lines 1-10; col. 10, lines 10-15; and col. 11, lines 1-20) are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a single instruction with an operation code and address values in its operand to Rahman's system because it would allow an instruction to influence multiple lines in a cache, invalidating an entire cache range, thereby reducing overall operation times. Milburn shows a decoder to decode an instruction (e.g., fig. 2, line 203) are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a decoder to Rahman's system because it would produce an operation and a address values of an instruction and it would allow an instruction to influence multiple lines in a cache, invalidating an entire cache range, thereby reducing overall operation times .

As per claims 5, 10, 40, 44, 48, 53-54, 58-59, Rahman shows the portion of a starting address including a plurality of most significant bits of the starting address (i.e., tag address; e.g., col. 7, line 22 and et seq.); Rahman does not specifically show execution unit shifts the data elements or portion of an address by a predetermined number of bits positions represent a number of least significant bits to obtain the starting address of the cache line in which data to be invalidated or copied. Even though Rahman teaches the use of validation being implemented through instruction in the CPU micro code stored in ROM and operating address values to invalidate or copy

data (e.g., col. 7, line 22 and et seq.) but does not specifically show the use of providing a single instruction with an operand and decoder to decode an instruction. Milburn shows providing a single instruction with an operation code and address values in its operand (e.g., col. 9, lines 1-10; col. 10, lines 10-15; and col. 11, lines 1-20) are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a single instruction with an operation code and address values in its operand to Rahman's system because it would allow an instruction to influence multiple lines in a cache, invalidating an entire cache range, thereby reducing overall operation times. Milburn shows a decoder to decode an instruction (e.g., fig. 2, line 203) are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a decoder to Rahman's system because it would produce an operation and a address values of an instruction and it would allow an instruction to influence multiple lines in a cache, invalidating an entire cache range, thereby reducing overall operation times. Official Notice is taken that both the concept and advantages of shifting the data elements or portion of an address by a predetermined number of bits positions are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have shifting the data elements by a predetermined number of bits positions to Rahman's system because it would allow rearrange an order of address bits in a particular sequence.

7. Applicants remarks filed 9/26/03, not deemed moot in view of the new grounds of rejection, have been considered but are not persuasive.

8. In the remarks, Applicants argue in substance that Rahman does not teach the user specified starting address or one skilled in the art would not perform the selectively invalidating using a single instruction of the processor instruction set, sine the instructions to perform such activity are not performed by the direction of a user.

The examiner respectfully disagrees as cited in the above office action, Rahman shows the user specified starting address (e.g., col. 3, lines 25-35 or abstract). In other word based on the citation above, Rahman teaches the software routines or instructions in microcode written by a user who specified the start address to compare to the tag address. The examiner would like to point out that Rahman not only teaches "selective invalidating of the cache memory in response to the removable, modification or disabling" the applicant's remarks filed 9/26/03, page 8, second paragraph), but also teaches a user specified starting invalidation address by the user removes or modifies or disables an external device to cause an invalidation of the corresponding start address of the external device. Therefore, Rahman does teach the user specified starting address or one skilled in the art would perform the selectively invalidating using a single instruction of the processor instruction set, sine the instructions to perform such activity are performed by the direction of a user.

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Bomba et al. (4648030) shows invalidating cache data within the address range of a write command;

b) Getzlaff et al. (55948760) shows a programmer keeps track of an addressed ranges for flushing;

c) Walters et al. (5768593) shows a partial cache flush instruction; and

d) Earl (6049866) shows an invalidating address range implemented directly from user mode.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Denise Tran whose telephone number is (703) 305-9823. The examiner can normally be reached on Monday, Thursday and an alternated Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone numbers for

the organization where this application or proceeding is assigned are (703) 872-9306 for central Official communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

D.T.
December 14, 2003